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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/190,618	11/12/1998	HONGYONG ZHANG	0756-1881	6863

31780 7590 08/19/2003

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EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/190,618	ZHANG ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25,34-39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25,34-39,41 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/312,795* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *40* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/25/03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 thru 4, 6 thru 9, 12 thru 14, 16 thru 22, 24, 25, 34 thru 38, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto '042 in view of Kunii et al. '493. Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor (first thin film transistor) 12 for a matrix circuit and a thin film transistor (second thin film transistor) 13 for a peripheral circuit. Each transistor comprises a gate electrode 25-27, gate insulating film 24, semiconductor thin film 21-23, channel regions 21a-23a, high level impurity source/drain regions (a pair of first regions) 21c-23c, and low level impurity source/drain regions (a pair of second regions) 21b-23b. The figure clearly shows the gate electrode overlapping the low level impurity source/drain regions. Matsumoto does not disclose the distance between the

channel forming region and the pair of first regions of said first thin film transistor being greater than that of said second thin film transistor. However it was well known in the art at the time of invention that active matrix pixel TFTs were susceptible to charge leakage. See, for example, column 13, line 46-61. Therefore it would have been obvious to one of ordinary skill in the art at time of invention to increase the length of the low level impurity region (and therefore increase the distance between the channel forming region and the pair of first regions) in the first thin film transistor in order to suppress charge leakage prevalent in the matrix pixel TFT.

a. Regarding claims 2 and 20, see, for example, column 4, line 40.

b. Regarding claims 3, 21, and 41 see, for example, column 5, line 31-55.

c. Regarding claims 6 thru 9, 17, 24, 25, 34, and 35, Matsumoto does not specifically disclose a distance between the channel regions and high level impurity source/drain regions (pair of first regions) within a range of 0.4 to 2 um. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use these specific distances since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980). Also, see ***Prior Art*** paragraph below.

d. Regarding claims 24, 25, 34, and 35, Matsumoto discloses the claimed invention except for the specific impurity concentrations of the first and second regions. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use these impurity concentrations since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

e. Regarding claim 37 and a pixel electrode, see element 28 in FIG. 1.

4. Claims 5, 10, 15, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto '042 in view of Kunii et al. '493 as applied to claims 1 thru 4, 6 thru 9, 12 thru 14, 16 thru 22, 24, 25, 34 thru 38, 41 and 42 above, and further in view of Dohjo et al. '551. Matsumoto in view of Kunii does not disclose the gate electrode as having a multi-layered structure consisting of aluminum, tantalum, titanium or silicon. However, Dohjo et al. '551 teaches that the gate electrode may contain multiple layers that consist of, for example, tantalum. See, for example, figure 7. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a multi-layered structure gate electrode in order to improve the resistivity of the gate electrode as taught by Dohjo et al. (see, for example, column 9, line 43 and Table on columns 5 and 6).

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto '042 in view of Kunii et al. '493 as applied to claims 1 thru 4, 6 thru 9, 12 thru 14, 16 thru 22, 24, 25, 34 thru 38, 41 and 42 above, and further in view of Lee 5,430,320. Matsumoto in view of Kunii does not disclose an insulating film comprising silicon oxide over the gate electrode. However, Lee discloses a thin film transistor comprising silicon oxide films 16, 17 over a gate electrode 15. The silicon oxide films protect the gate electrode and insulate the gate electrode from subsequent layers. The silicon oxide also serves as a good material for making via holes. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the silicon

oxide in Matsumoto in view of Kunii in order to adequately protect the gate electrode from other layers and also as a material to form via holes in.

6. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto '042 in view of Kunii et al. '493 as applied to claims 1 thru 4, 6 thru 9, 12 thru 14, 16 thru 22, 24, 25, 34 thru 38, 41 and 42 above, and further in view of Iizuka '269 A. Matsumoto in view of Kunii does not disclose said second impurity regions containing one of carbon, nitrogen, and oxygen at a higher concentration than said first impurity regions. However, Iizuka discloses that doping a polycrystalline Si layer with O or N ions will increase the resistivity. Since it was well known in the art at the time of invention that LDD regions require a high resistance (see, ***Prior Art*** paragraph below), it would have been obvious to one of ordinary skill in the art at the time of invention to dope the low level impurity regions of Matsumoto in view of Kunii so that one can increase its resistance and decrease the electric field concentration near the drain region.

Prior Art

7. The prior art is made of record and not relied upon is considered pertinent to applicant's disclosure. See, for example, column 14, lines 2-7 where Kunii et al. states the dimensions (i.e. the length of an LDD is 1um) of a conventional thin film transistor. See also column 13, lines 37-61 where Kunii states various lengths of the lightly doped region; all lengths within the 0.4 to 2 um range stated in the claims.

8. The prior art is made of record and not relied upon is considered pertinent to applicant's disclosure. See, for example, column 33, lines 28-46 where Miyasaka et al. '957 B1 states the presence of a high resistance region removes a concentrated electric field at the drain edge of a channel.

Response to Arguments

9. Applicant's arguments filed 7/25/03 have been fully considered but they are not persuasive.

The new limitation "a distance between edges of the channel forming region and edges of the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor" is no different than stating that the first TFT (in the active matrix) has a larger low level impurity region than the low level impurity region in the second TFT (in the driving circuit).

Kunii clearly states (see column 13, lines 46-61) that increasing the length of the low level impurity region in the matrix pixel TFT will suppress the charge leakage in the matrix pixel TFT. Therefore, by increasing the length of the low level impurity region in the matrix pixel TFT, the length of the low level impurity region in the matrix pixel TFT will be greater than the low level impurity region in the driving circuit of Matsumoto. The TFT with the picture element electrode 13 has a low level impurity region with a greater length (1.5 um) than the TFT without the picture element electrode (1 um).

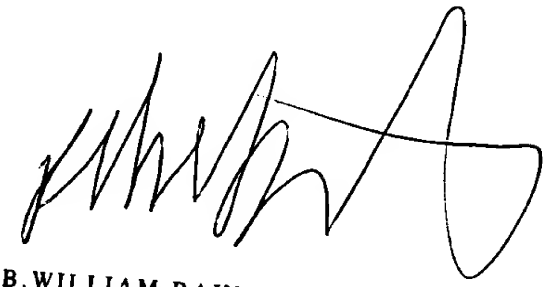
INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
August 10, 2003



B. WILLIAM BAUMEISTER
PRIMARY EXAMINER